PhD proposal

Signal processing on stochastic architecture: a GPS case study.

Lab-STICC
Université de Bretagne Sud
Director : Prof. Emmanuel Boutillon

One of the most critical challenges of the ITRS overall design technology (2010) is fault-tolerant computation. The increase in integration density and the requirement of low-energy consumption can only be sustained through low-powered components, with the drawback of a looser robustness against transient errors. In the near future, electronic gates to process information will be inherently unreliable. The Labex CominLab (excellence center) funds the RELIASIC project on this topic (2014-2017).

The RELIASIC will address this problem with a bottom-up approach, starting from an existing application (a GPS receiver) and adding some redundant mechanisms at the hardware level to allow the GPS receiver to be tolerant to transient errors due to low voltage supply. The objective of this PhD is to demonstrate non-conventional methods at the architecture level to protect vital signal processing functions of a GPS receiver against internal errors.

More information on the RELIASIC project available at:
http://www-labsticc.univ-ubs.fr/~boutillon/un_arch/un_arch.html

State of the art

Research on computation on unreliable computing is as old as electronics. In fact, Von Neuman has proposed a theoretical solution to the problem in 1956 [2]. The idea is to use a set of N wires to represent a given information. Logic functions are also duplicated N-times. Then a restoration process is applied to reduce the error probability of the output functions. The restoration process triplicates each function output to generate 3N wires, which are interleaved in a random way. A new N-wire signal is then reconstructed using N noisy 3-input majority gates. If the error probability of the function and the 3-majority gate is low enough (NAND gate with a probability of error around 0.01), perfect computation can be performed when N goes towards infinity. The problem of this method is that the hardware

efficiency (the average amount of computation per time unit and area unit) goes towards zero, which is not acceptable in practice.

Over almost 60 years, the problem of computation on unreliable architecture has been studied, Mostly for applications working in high radiation environment (e.g. space and nuclear applications) and/or requiring very high level of reliability (e.g. aircraft control). Recently, the area of fault tolerant computation has spread in general purpose applications. In "Error-resilient systems via statistical signal processing," [3], R. Abdallaf and N. Shanbhag present a very interesting survey of modern fault tolerant techniques. They claim potential savings of 3 to 6× in energy thanks to an efficient integration of redundancy in few critical parts of a digital design.

Objectives of the thesis

The PhD student will develop unconventional methods to perform signal processing computation on unreliable hardware. Those unconventional methods will include stochastic computation, hybrid dual module systems, and residue and redundant number systems.
Based on the result of the thesis (an others contributions of the RELIASIC project), an ASIC will be designed to compare theoretical results and measured results.

Background:

To apply to this PhD, you should have a master degree and background in signal processing, error control coding and digital implementation. Knowing a hardware language for modelling and synthesis will be also useful (VHDL, Verilog or System C).

Contact :

Professor Emmanuel Boutillon
Lab-STICC (http://www.lab-sticc.fr/)
Université de Bretagne Sud
Mail: Emmanuel.boutillon@univ-ubs.fr
Tel: 02 97 87 45 66
Web page: http://www-labsticc.univ-ubs.fr/~boutillon/anglais.html